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To: Examiner Long K. Tran	Total Pages Sent: 2
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Facsimile Number: 703-872-9306	Transmission Date: June 22, 2005

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**


Applicants: Schloesser, et al. Docket No.: INF-135  
Serial No: 10/777,128 Art Unit: 2818  
Date Filed: February 13, 2004  
Title: Method of Fabricating and Architecture for Vertical Transistor Cells and Transistor-Controlled Memory Cells

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- Certification of Facsimile Transmission (1 page)
- Election (1 page)

Respectfully submitted,

  
AnneMarie James  
Legal Assistant

Confirmation Respectfully Requested

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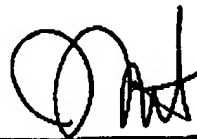
Mail Stop Amendment  
Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

**ELECTION**

Dear Sir:

In response to the restriction requirement set forth in the Office Action mailed on May 26, 2005, the Applicants hereby elect Group I (Claims 1-19) for further prosecution in the above patent application.

Respectfully submitted,



Ira S. Matsil  
Attorney for Applicants  
Reg. No. 35,272

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